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A VERTICALLY INTEGRATED DYNAMIC RAM-CELL: BURIED BIT LINE MEMORY CELL WITH FLOATING TRANSFER LAYER

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Abstract—A charge injection device has been realized in which charge can be injected on to an MOS-capacitor from a buried layer via an isolated transfer layer. The cell is positioned vertically between word and bit line. LOCOS (local oxidation) is used to isolate the cells and (deep) ion implantation to realize the buried bit line and transfer layer. This isolation prevents carriers from diffusing to neighbouring cells and hence preserves stored information. The device physics has been analysed using simulation programs and bipolar modelling. It is shown that this device can be used as a dynamic RAM-cell of extreme simplicity and potentially small cell size compared to conventional DRAM cells.

INTRODUCTION

A buried bit line (BBL) memory cell is in essence a charge injection device (CID). Charge carriers can be injected from a buried layer via punch-through of a transfer layer on to a MOS capacitor, where they constitute an inversion layer as in Fig. 1.

The stored charge can be injected back to the buried layer via punch-through in the opposite direction by pulsing the MOS-gate appropriately.

A three-terminal charge injection device was first proposed as a dynamic RAM cell by Koch *et al.*[1] and later reviewed in the survey of Chatterjee[2]. In [1] a CID-cell which was originally intended for imaging applications, was modified into a DRAM cell by suppressing the "blooming-effect"—cross-talk between neighboring imaging cells—through the use of an epi-layer. In work reported later by Grassl *et al.*,[3], this suppression was shown to be insufficient and other ways were explored. In this paper, a solution is presented to the unwanted stray carriers by totally isolating the transfer layer from the bulk, and hence from other cells. Deep ion implantation, combined with LOCOS isolation, is an appropriate means to realize this structure by a relatively simple process (see Fig. 2).

The process contains seven masks. The first mask defines LOCOS areas, and a second is needed to define the 1-MeV phosphorus implants. The transfer layer is realized using an unmasked implant. A mask is needed to define the contact implants to the bit line and source and drains of peripheral circuits. Contact holes, metallization and scratch protection each require one mask. In a memory matrix organization the gates are row-wise connected as word lines and the buried implanted layers column-wise as bit lines. Full selection takes place when both word and bit line are activated. If only one of these lines is activated a cell is half selected.

Because of the now isolated transfer layer the device analysis will differ slightly from that of the CID-cell. The high-energy phosphorus implant does not allow a high implant dose. As an undesirable result the sheet resistance of the bit line is relatively large. The bit line capacitance, however, is kept small because the tail of the profile of the implanted buried n-layer constitutes a relatively wide depletion layer. The implant dose of the transfer layer can be adjusted so as to give appropriate operating voltages and to limit electrical field strengths to below a critical level. Since the leading edge of the impurity distribution of the implanted phosphorus layer is not very steep, increasing the phosphorus implant to decrease bit line resistance will also require a higher dose for the transfer-layer implant, thereby increasing operating voltages and electric fields. Using SUPREM[4] and SEDAN[5] simulations, this trade-off has been analysed.

OPERATION OF THE BURIED BIT LINE MEMORY CELL

For a qualitative description of the operation of the BBL-cell we refer to Fig. 3(a) and (b).

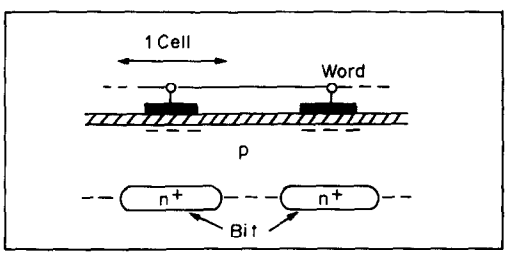

Fig. 1. Basic CID-cell.

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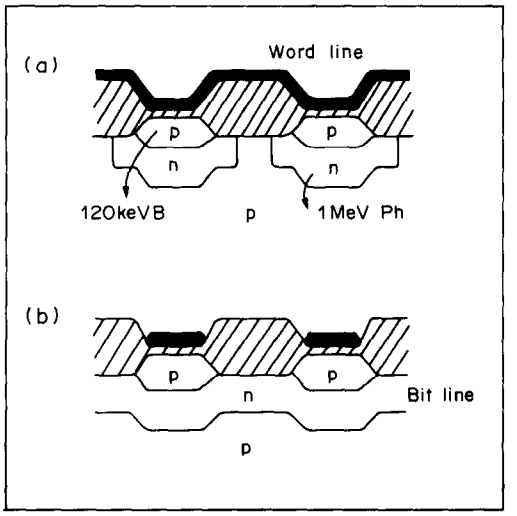

Fig. 2. Buried-bit line CID cell realized with deep ion implantation and LOCOS isolation. (a) Cross-section along the word line, (b) along the bit line.

Only two electrical contacts are of interest to the cell: the gate (word line) and the bit line. The bulk can be given a negative voltage to reduce bit line–bulk capacitance. The bulk is considered the reference electrode. The cell is considered to be in a logical "0" condition when electrons are stored under the MOS capacitor. The logical "1" refers to the absence of an inversion layer. Charge can be written into the cell by keeping the bit line at zero potential and pulsing the word line positive in order to inject electrons from the bit line across the transfer layer to the Si–SiO_2 interface. During storage, both word and bit lines are at intermediate levels where the flow of electrons across the transfer layer is blocked. Charge can be read out from the cell by holding the bit line at positive potential and pulsing the word line negative. The transfer layer will act as a base of an *npn* transistor, and electrons from the inversion layer flow as collector current to the bit line. Reading is destructive. Figure 3(b) shows the potential distribution in the device under the various conditions and defines the different parameters. ϕ_b and ϕ_0 are the built-in potentials of the bit line–substrate and bit line–transfer layer junctions respectively. Figure 4 shows measured pulse shapes on experimental BBL-cells during reading and writing of both "0" and "1", as well as voltage conditions on half-selected cells in matrix operation. In an actual memory matrix reading can be achieved by comparing the bit line current to the current of a reference cell, and latching a difference.

During reading all cells connected to the selected word line will be read. Peripheral circuitry has to perform the selection and all cells on the word line have to be refreshed. For the peripheral circuits N-MOS transistors can be realized with an extra mask for the implantation of the threshold adjust.

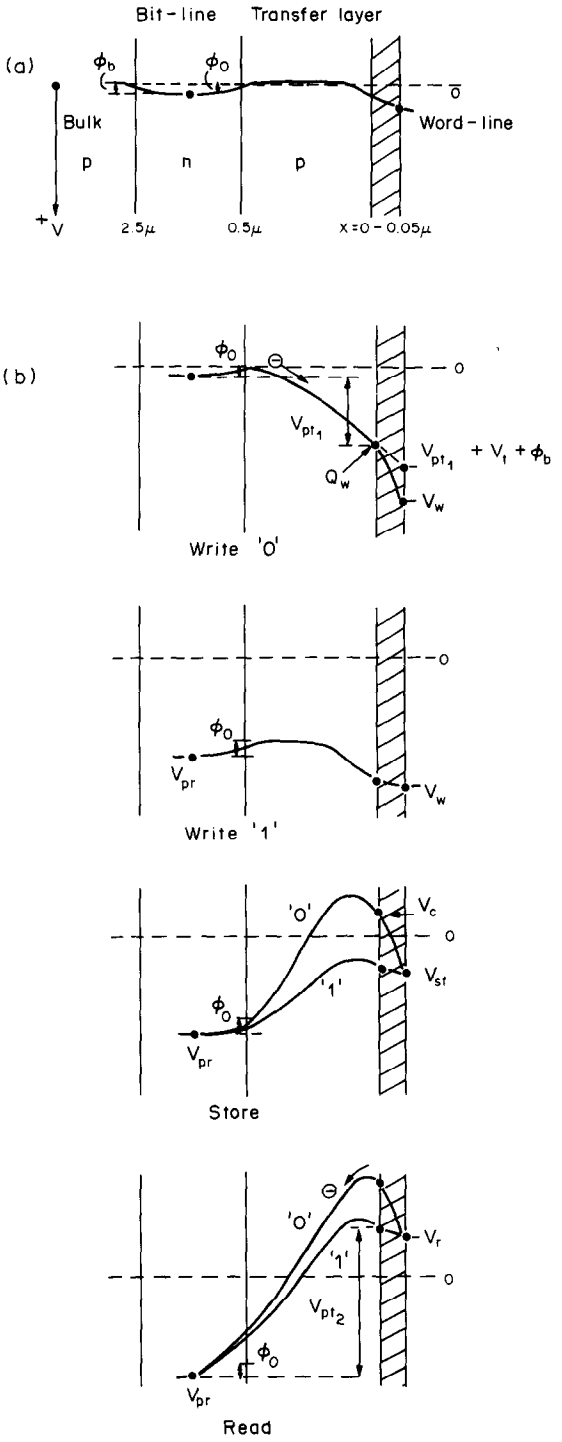

Fig. 3. (a) Cross-section through active device under zero bias. ϕ_b is the built-in potential of the bit line–substrate junction and ϕ_0 the built-in potential between bit line and transfer layer. (b) Various biasing conditions for writing and reading. V_w, V_{st} and V_r are the word line voltages for writing, storing and reading respectively. V_{pr} is the pre-charge level voltage of the bit line. V_{pt1} and V_{pt2} are punch-through voltages between the inversion layer at the Si–SiO_2 interface and the bit line under opposing biasing conditions. Q_w is inversion layer charge and V_f the potential drop across the oxide at the onset of inversion. The potential in the substrate is the reference level.

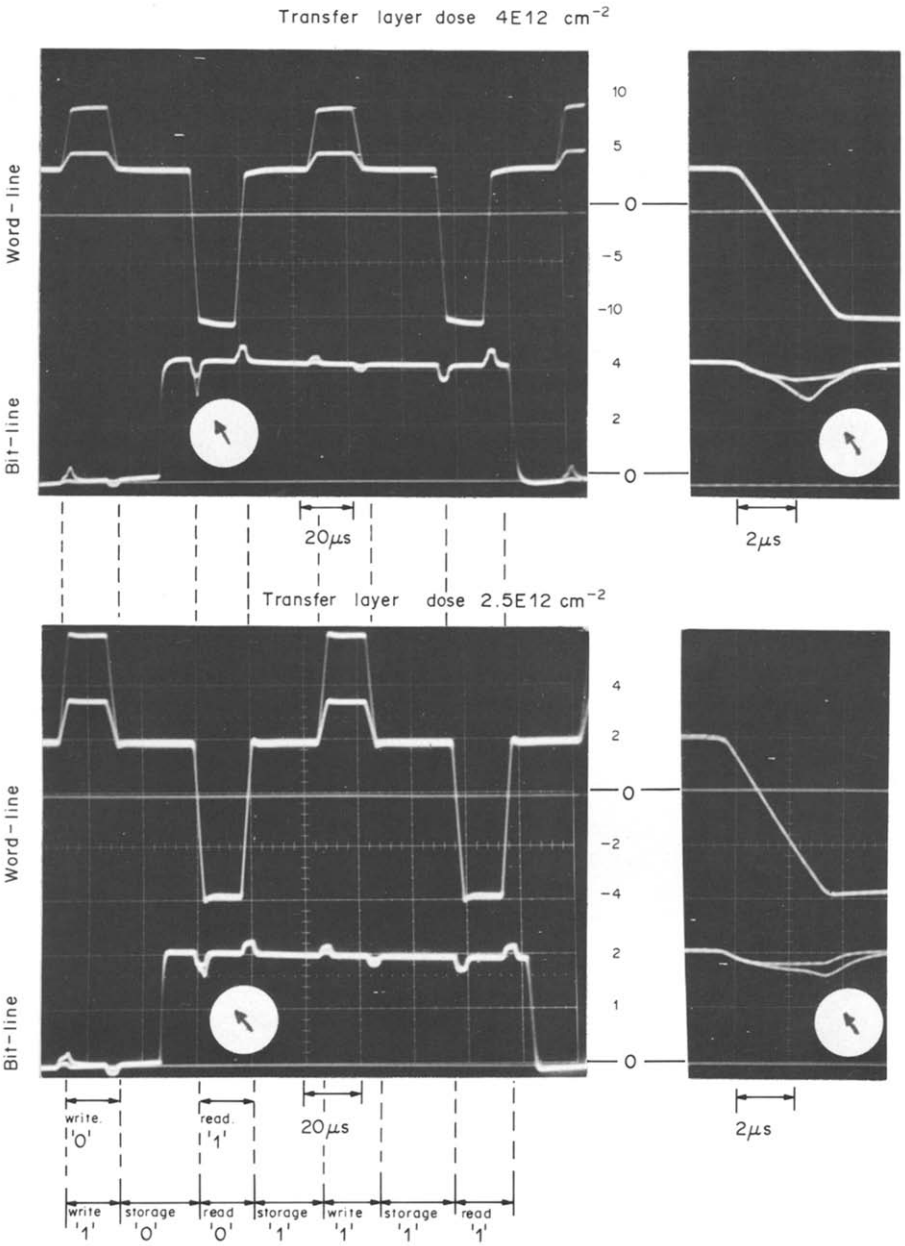

Fig. 4. Pulse shapes at two experimental cells with different transfer layer implant doses. Two word line voltages are applied with different amplitudes during writing. When the bit line is high, reading is achieved to built up inversion charge. The different reading pulses are shown on an enlarged time-scale also. The bit line voltage was measured across a load resistance of 4.7 kΩ.

Except for an anneal step no extra processing is needed.

When writing a "0", electrons can flow only if the transfer layer potential barrier is sufficiently lowered. The potential between the Si–SiO_2 interface and the bit line for which the onset of this electron injection is reached is defined as the punch-through voltage V_{pt1}. It is convenient in terms of device simulation to equate V_{pt1} here to that interface voltage where the Gummel number in the transfer layer is minimum. If the word line voltage for writing,

$$V_w > V_{pt1} + V_t + \phi_b, \tag{1}$$

an inversion layer forms, with V_t the potential drop across the oxide at the onset of inversion. If the fixed oxide charge is zero, V_t follows from the continuity of the dielectric displacement at the interface. It is evident that the charge written in the cell is

$$Q_w = -C_{ox}[V_w - (V_{pt1} + V_t + \phi_b)]. \tag{2}$$

For writing a "1", inversion must be prevented by rising the bit line voltage to a precharge level, V_{pr}, to

prevent punch-through. If

$$V_w - V_{pr} < V_{pt1} + V_t, \tag{3}$$

no inversion layer forms.

During storage the bit line is kept at V_{pr} to limit the number of different voltages needed for operation of the cell. The word line voltage V_{st} now must satisfy the condition that flow of electrons from the inversion layer to the bit line is prevented. The isolation of the transfer layer is an important factor in the analysis of storage and reading. The bulk cannot act as a source or sink for holes when writing has finished and storage or reading starts, contrary to a traditional CID-cell. To find the conditions for the storage and reading voltages one has to take into account the dynamics of the thermal generation in the transfer layer.

During the write cycle the transfer layer is at least partially depleted of holes, and since the flow of holes from the substrate to the transfer layer is blocked by the reverse biased bit line, thermal generation is the only supply of holes to restore the equilibrium concentration when writing has finished. This is a process with a relatively long time constant. The thermal generation rate roughly is 10^{16} s^{-1} cm^{-3}. Since the Gummel number in the transfer layer is in the order of 10^{12} cm^{-2} and the layer thickness is 0.5 μm, it will take 2 s to completely regenerate the hole concentration. It is therefore reasonable to assume that the transition time from a writing action to storage is much shorter than the time needed to completely regenerate the transfer layer.

After writing, the word line voltage can be set to a value V_{st} that still accommodates the actual number of holes present in the transfer layer. Setting it to a lower value would mean the loss of inversion charge. The lower limit of V_{st} hence depends on the time interval between writing and storage and can in practice be in the order of V_{pr} or even lower. The maximum value is set by the condition

$$V_{st} < V_{pt1} + V_t + \phi_b, \tag{4}$$

since one should not write into cells half selected by the bit line.

The voltage necessary for reading also principally depends on the actual hole density in the transfer layer and hence the time interval between writing and reading. If the transfer layer is partially regenerated, the word line voltage only has to be lowered to a value slightly below the value that can still accommodate the number of holes present in the transfer layer to cause the loss of inversion charge. The inversion layer then is forward biased with respect to the transfer layer, and electrons from the inversion layer are injected to the thin transfer layer and will be collected by the bit line.

If the transfer layer is still fully depleted the word line-to-bit line voltage necessary for reading will be equal to the punch-through voltage between inversion layer and bit line, V_{pt2}. Since in practice some thermal generation will have taken place in the time interval between writing and reading, reading will certainly take place when the reading voltage V_r is conditioned as

$$V_{pr} - [V_r - (V_t + \phi_b)] > V_{pt2}. \tag{5}$$

QUASI-STATIC ANALYSIS OF PUNCH THROUGH USING BIPOLAR MODELLING

If doping concentrations are constant, an analytical solution of Poisson's equation for the different conditions of Fig. 3(b) is possible[3], but here ion implantation will result in relatively steep profiles, and the use of computer simulation is apparent.

The implantation profile of the cross-section through the active device is as shown in Fig. 5. The profile is determined using SUPREM, where implantation profile parameters have been adjusted with recently available data[6,7]. A large deviation between the results of CV-profiling and simulation of the leading edge of the phosphorus implant has been found. This deviation is due to the inaccurate profile parameters available up to now and possibly incomplete modelling of damage-enhanced diffusion at low temperatures after implantation.

Since only two contacts are available to the cell and the potential in the inversion layer will be determined by the potential on these contacts only, normal MOS device simulation can not be used. To determine the onset of punch-through between channel and bit line, V_{pt2}, the potential distribution can be analysed using bipolar transistor simulation with SEDAN by assuming a thin n-layer (inversion layer) at the Si–SiO_2 interface as emitter, the transfer layer as base and bit line as collector. The punch-through voltage is defined as the emitter–collector voltage for which the Gummel number (active charge density) in the transfer layer is minimum. The V_{pt2} thus found is relatively insensitive to the value of the electron concentration assumed in the inversion layer as long as it is higher than the peak concentration in the transfer layer. As soon as the Gummel number drops significantly, SEDAN will indicate a static current. In the actual device, a current will reduce the concentration in the inversion layer and hence the built-in potential between inversion layer and transfer layer. This indicates that the inaccuracy in the determination of V_{pt2} is a few hundred millivolts.

V_{pt1} can be found in the same way, considering the bit line as emitter and channel as collector. Although a channel is already assumed in this simulation using a bipolar model, the punch-through voltage found is correct with the same accuracy as V_{pt2}, since in the simulation a stationary current will flow out the collector terminal that in the actual device precisely causes the inversion.

To simulate the behaviour of the actual device as closely as possible, the profile parameters of the 1-MeV phosphorus implant used in SUPREM were

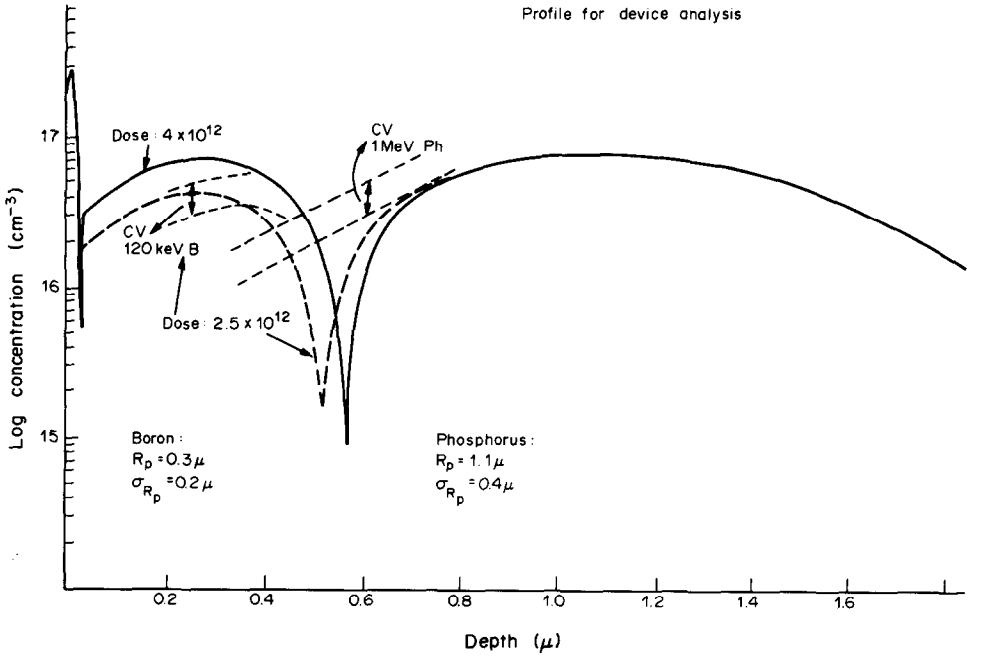

Fig. 5. Net concentration profiles of two experimental cells used as input for device simulation. The thick solid and dashed lines are SUPREM II results while the thin dashed lines indicate the range of the CV measurement results for the two implants separately.

adjusted to yield a concentration profile close to the CV measurement results. A channel with 3×10^{12} electrons/cm^2 was assumed in a layer of *ca.* 5×10^{-3} μm thick. Gummel numbers in the transfer layer are plotted vs inversion layer-to-bit line voltage in Fig. 6.

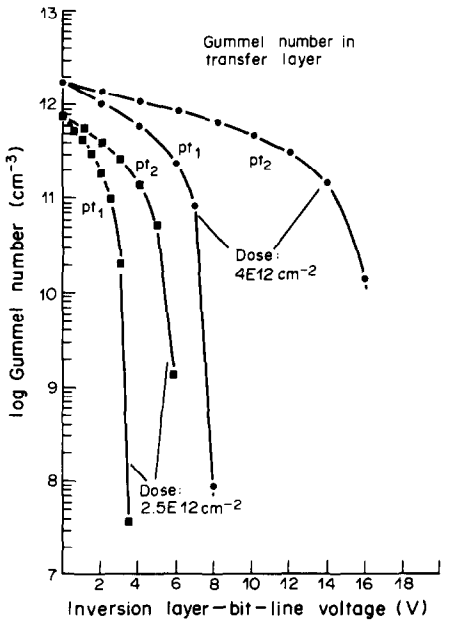

Fig. 6. Gummel number in transfer layer as function of channel–bit line voltage for the two experimental cells for both writing (*pt*1) and reading (*pt*2) situations

Since the electric field strengths are rather large in the device with a transfer layer implant dose of 4×10^{12} cm^{-2}, one can expect avalanche breakdown to occur before actual punch-through. If this occurs during reading, no harm is done, but when writing, one can create hot electrons which could be injected into the oxide. The boron dose can be decreased to prevent this. Figure 7 shows boron implant dose vs V_{pt}.

MEASUREMENTS AND DISCUSSION

From the simulation results we can conclude that for the experimental cells with transfer layer dose of

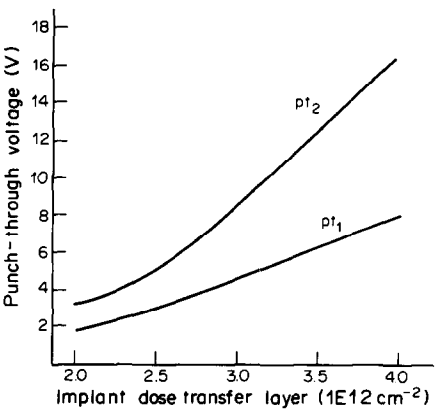

Fig. 7. Both punch-through voltages as a function of transfer layer implant dose.

$4 \times 10^{12}\,cm^{-2}$, $V_{pt1} = 8$ V and $V_{pt2} = 17$ V; with transfer layer dose of $2.5 \times 10^{12}\,cm^{-2}$, $V_{pt1} = 3$ V and $V_{pt2} = 5$ V. Comparing these results with the obtained pulse shapes of Fig. 4, it can be concluded that the operating voltages used correspond to the conditions set by Fig. 3(b) and the values of punch-through voltages found. The pulse shapes of Fig. 4 were measured on a test cell of $300 \times 300\,\mu m^2$ in order to obtain acceptable signal levels. The bit line signal was measured across a 4.7 kΩ resistor between bit line and virtual ground, using a 10 pF capacitive loading from the oscilloscope probe.

It has been shown that the principle of the CID can be extended to a BBL-device with a floating transfer layer, and that the analysis of device operation is rather simple. To use the merits of the BBL-cell in a dynamic memory matrix, the high bit line sheet resistance (1.4 kΩ/sq for the experimental cells) has to be lowered, either by using epi-wafers with extra buried n^+ layers to contact the implanted bit lines or increasing the cell pitch and running an n^+ layer parallel to the bit line. The apparent advantages of the proposed DRAM-cell are the extremely small size, simple processing and also high yield potential since no contact windows are needed in the memory matrix. The critical step is the boron transfer layer implant. Any particles present on the cells will cause weak spots in the transfer layer. Reading and writing speed of a memory largely depends on the transmission behaviour of word and bit lines since carrier transport in the memory cells is extremely fast.

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